IN THE CLAIMS:

1. (Currently Amended) A built-in self-test controller, comprising:

a plurality of alternative memory built-in self-test state machines; ~~and~~

a memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines; and

a logic built-in self-test engine;

wherein the built-in self-test controller is geographically centralized within an integrated circuit.

2. (Cancelled).

3. (Previously Presented) The built-in self-test controller of claim 1, further comprising a memory built-in self-test signature generated by an execution of the memory built-in self-test.

4. (Cancelled).

5. (Previously Presented) The built-in self-test controller of claim 3, wherein the memory built-in self-test signature includes a bit indicating whether a memory built-in self-test is done.

6. (Original) The built-in self-test controller of claim 1, wherein at least one of the memory built-in self-test state machines comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state upon completing a flush of a plurality of memory components to a known state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

7. (Currently Amended) A built-in self-test controller, comprising:

means for implementing a plurality of states in a plurality of sets in a memory built-in self-test; ~~and~~

means for operating a predetermined one of the sets in the memory built-in self-test; and

a logic-built-in self-test engine

wherein the built-in self-test controller is geographically centralized within an integrated circuit.

8. (Cancelled).

9. (Previously Presented) The built-in self-test controller of claim 7, further comprising a memory built-in self-test signature generated by an execution of the memory built-in self-test.

10. (Original) The built-in self-test controller of claim 7, wherein at least one of the sets comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state upon completing a flush of a plurality of memory components to a known state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

11. (Currently Amended) An integrated circuit device, comprising:

a plurality of memory components;

a testing interface; and

a built-in self-test controller controlled through the testing interface, comprising:

a logic built-in self-test engine;

a plurality of alternative memory built-in self-test state machines; and

a memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines, wherein the built-in self-test controller is geographically centralized within the integrated circuit device.

12. (Cancelled).

13. (Previously Presented) The integrated circuit device of claim 11, further comprising a memory built-in self-test signature register generated by an execution of the memory built-in self-test.

14. (Cancelled).

15. (Previously Presented) The integrated circuit device of claim 13, wherein the memory built-in self-test signature includes a bit indicating whether a memory built-in self-test is done.

16. (Original) The integrated circuit device of claim 11, wherein at least one of the memory built-in self-test state machines comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state upon completing a flush of a plurality of memory components to a known state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

17. (Previously Presented) The integrated circuit device of claim 11, wherein the memory com ponents include a static random access memory device.

18. (Original) The integrated circuit device of claim 11, wherein testing interface comprises a Joint Test Action Group tap controller.

19. (Currently Amended) An integrated circuit device, comprising:
a plurality of memory components;
a testing interface; and
a built-in self-test controller controlled through the testing interface, comprising:
a logic built-in self-test engine;
means for implementing a plurality of states in a plurality of sets in a memory built-in self-test, wherein the built-in self-test controller is geographically centralized within the integrated circuit device; and
means for operating a predetermined one of the sets in the memory built-in self-test.

20. (Cancelled).

21. (Original) The integrated circuit device of claim 19, further comprising a memory built-in self-test signature register generated by an execution of the memory built-in self-test.

22. (Original) The integrated circuit device of claim 19, wherein at least one of the sets comprises:
a reset state entered upon receipt of an external reset signal;
an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state upon completing a flush of a plurality of memory components to a known state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

23. (Previously Presented) The integrated circuit device of claim 19, wherein the memory components include a static random access memory device.

24. (Original) The integrated circuit device of claim 19, wherein testing interface comprises a Joint Test Action Group tap controller.

25. (Currently Amended) A method for performing a built-in self-test on an integrated circuit device, comprising:

externally resetting a predetermined one of a plurality of memory state machines in a memory built-in self-test controller, wherein the memory built-in self-test controller is geographically centralized within the integrated circuit;

performing a memory built-in self-test utilizing the ~~the~~ one of the plurality of memory state machines

externally resetting a logic state machine;

performing a logic built-in self-test utilizing the logic state machine; and

obtaining the results of the performed logic built-in self-test; and

obtaining the results of the performed memory built-in self-test.

26. (Previously Presented) The method of claim 25, wherein performing the memory built-in self-test includes:

initiating a plurality of components and signals in a memory built-in self-test domain of the memory built-in self-test controller upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals in the memory built-in self-test domain; and

testing the flushed memory components.

27. (Previously Presented) The method of claim 26, wherein performing the memory built-in self-test further includes at least one of:

storing the results of the memory built-in self-test in a memory built-in self-test signature register;

setting a bit in the memory built-in self-test signature register indicating whether the memory built-in self-test is done.

28. (Cancelled).

29. (Original) The method of claim 25, wherein obtaining the results includes receiving the results as the memory built-in self-test is performed or reading the stored results from a register.

30. (Currently Amended) A method for testing an integrated circuit device, comprising:

interfacing the integrated circuit device with a tester;

externally resetting a built-in self-test controller, including:

externally resetting a predetermined one of a plurality of memory state machines; and

externally resetting a logic state machine;

performing a logic built-in self-test from the built-in self-test controller;

performing a memory built-in self-test from the built-in self-test controller; and

obtaining the results of the performed memory built-in self-test;

wherein the built-in self-test controller is geographically centralized in the integrated circuit device.

31. (Previously Presented) The method of claim 30, wherein performing the memory built-in self-test includes:

initiating a plurality of components and signals associated with the memory built-in self-test upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after the initialization of the associated components and the signals; and

testing the flushed memory components.

32. (Original) The method of claim 31, wherein performing the memory built-in self-test further includes at least one of:

storing the results of the memory built-in self-test in a memory built-in self-test signature register;

storing the results of at least one paranoid check in the memory built-in self-test signature register;

setting a bit in the memory built-in self-test signature register indicating whether the memory built-in self-test is done.

33. (Original) The method of claim 30, wherein obtaining the results includes reading a memory built-in self-test signature.

34. (Original) The method of claim 30, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols.

35. (Cancelled).

36. (Original) The method of claim 30, wherein obtaining the results includes receiving the results as the memory built-in self-test is performed or reading the stored results from a register.